Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS**

1. **Q1**
2. **N. Q1**
3. **CLOCK 1**
4. **RESET 1**
5. **D1**
6. **SET 1**
7. **VSS**
8. **SET 2**
9. **D2**
10. **RESET 2**
11. **CLOCK 2**
12. **Q2**
13. **VDD**

**2 1 14 13 12**

**11**

**10**

**9**

**3**

**4**

**5**

**6 7 8**

**CD**

**4013BA**

**DIE ID**

**.050”**

**.050”**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .003” X .003”**

**Backside Potential: VDD**

**Mask Ref: CD4013BA**

**APPROVED BY: DK DIE SIZE .050” X .050” DATE: 9/20/21**

**MFG: TEXAS INSTRUMENTS**   **THICKNESS .025” P/N: CD4013BH**

**DG 10.1.2**

#### Rev B, 7/19/02